What is claimed is:

1. A general purpose state machine comprising:

a first plurality of external input terminals for receiving information from an external circuit;

a first multiplexer having a plurality of input terminals, at least some of which are coupled to the external input terminals to receive the information therefrom, the first multiplexer supplying a first output signal;

a programmable memory storing a plurality of words, each word having a plurality of bits, a word from the memory being supplied in response to an address signal;

a control circuit connected to receive the output signal from the first multiplexer and connected to receive a first set of bits from a word in the programmable memory, the control circuit providing a signal selecting one of the words in the programmable memory; and

wherein the external circuit is connected to receive at least a second set of bits from the same word of the programmable memory as the first set of bits in response to selection of a word by the control circuit.

2. A general purpose state machine as in claim 1 further comprising a decoder coupled between the control circuit and the programmable memory, wherein the decoder is coupled to receive the signal from the control circuit, decode that signal, and thereby provide the address signal to select the word to be supplied by the programmable memory.

3. A general purpose state machine as in claim 2 further comprising a register connected between the decoder and the control circuit to temporarily store the signal from the control circuit selecting one of the words in the programmable memory.

4. A general purpose state machine as in claim 2 wherein the control circuit is coupled to also receive as an input signal, an address of a word previously selected.

5. A general purpose state machine as in claim 1 wherein the first set of bits received by the control circuit represents an address of a single word in the programmable memory.

6. A general purpose state machine as in claim 5 wherein the signal from the control circuit selects between the address provided by the first set of bits and the address of the word previously selected.

7. A general purpose state machine as in claim 5 wherein the first set of bits received by the control circuit represents addresses of two different words in the programmable memory.

8. A general purpose state machine as in claim 7 wherein:

the control circuit is coupled to also receive as an input signal, an address of a word previously selected; and

the control circuit selects among the two addresses represented by the first set of bits and the address of the previously selected word.

9. A general purpose state machine as in claim 1 wherein the input terminals of the first multiplexer are also connected to receive a third set of bits from the programmable memory.

10. A general purpose state machine as in claim 9 further comprising a second multiplexer having input terminals connected to each of the external input terminals, connected to the programmable memory to receive a fourth set of bits therefrom, and connected to provide an output signal to the control circuit.

11. A general purpose state machine as in claim 1 further comprising programmable logic coupled to at least some of the external input terminals and coupled to the first multiplexer to process information from the external circuit before it is provided to the first multiplexer.

12. A general purpose state machine as in claim 11 wherein the programmable logic comprises:

a first plurality of multiplexers connected in parallel to a plurality of external input terminals to provide a corresponding first plurality of output lines, each of the first plurality of multiplexers having a plurality of input terminals, each one of which is coupled to one of a first potential source and a second potential source; and

a second plurality of multiplexers also connected in parallel to the plurality of external input terminals to provide a corresponding second plurality of output lines, each of the second plurality of multiplexers having a plurality of input terminals, each one of which is coupled to one of the first potential source and the second potential source.

13. A general purpose state machine as in claim 1 further comprising at least one counter coupled to at least some of the external input terminals and coupled to the first multiplexer to process information from the external circuit before it is provided to the first multiplexer.

14. A general purpose state machine as in claim 1 further comprising at least one flag circuit coupled to at least some of the external input terminals and coupled to the first multiplexer to process information from the external circuit before it is provided to the first multiplexer.

15. A general purpose state machine as in claim 10 further comprising programmable logic coupled to at least some of the external input terminals and coupled to the second multiplexer to process information from the external circuit before it is provided to the second multiplexer.

16. A general purpose state machine as in claim 14 further comprising at least one counter coupled to at least some of the external input terminals and coupled to the second multiplexer to process information from the external circuit before it is provided to the second multiplexer.

17. A general purpose state machine as in claim 10 further comprising at least one flag circuit coupled to at least some of the external input terminals and coupled to the second multiplexer to process information from the external circuit before it is provided to the second multiplexer.

18. A general purpose state machine comprising:

a programmable memory storing a plurality of words, each word having a plurality of bits, a word from the memory being supplied in response to an address signal;

a control circuit coupled to receive at least first and second address signals from a word in the programmable memory, and coupled to receive signals from an external

circuit, control circuit selecting one of the first address or the second address in response to the signals from the external circuit; and

wherein by selection of one of the address signals, the control circuit implements one of an unconditional branch operation or a two-way conditional branch operation.

19. A general purpose state machine as in claim 17 wherein:

the control circuit is also coupled to receive a third address signal representing a previously addressed word; and

by selection of one of the address signals, the control circuit implements one of an unconditional branch operation, a two-way conditional branch operation, a three-way conditional branch operation, or a wait until conditional branch operation.